14.5 A 65nm C64x+™ Multi-Core DSP Platform for Communications Infrastructure

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The combination of the processing power of multiple 1.1GHz DSP cores and 65nm technology integration delivers the first WCDMA macro base-station on a single chip. The implementation of the signal-processing communications infrastructure platform illustrated in Fig. 14.5.1, supports Release 99, HSDPA and HSUPA (High Speed Downlink/Uplink Packet Access) standards with 3 DSP cores, symbol rate, and chip rate accelerators. Up to 64 users can be supported depending on the complexity of the WCDMA modem algorithms. The DSP MIPS can be allocated to symbol rate or chip rate assist processing or to trade-off processing for search and preamble detect correlation against finger despread processing. The on-chip WCDMA processing for the uplink to the Radio Network Controller (RNC) and downlink from the RNC to the Antenna interface is shown in Fig. 14.5.2. Software programmability allows flexibility in code partitioning to enable the platform to be used efficiently for applications handling a range of cell sizes and traffic scenarios. High-bandwidth focused peripherals, like serial Gigabit Ethernet, OBSAI (Open Base Station Standard Initiative) and CPRI (Common Public Radio Interface) compliant antenna interfaces, and 32b DDR2-667 allow the device to be connected flexibly. Data can be transported onto the board with Ethernet and with Antenna interface SERDES. Two lanes of Serial RapidIO at 3.125Gb/s provide chip-to-chip communication, directly or via a switch fabric to connect multiple DSPs. This architecture can cost-effectively support multiple standards like WiMax (Worldwide Interoperability for Microwave Access), TDSCDMA (Time Division Synchronous Code Division Multiple Access), EVDO and GSM. A combination of integration of antenna interface, software flexibility for code partitioning, multiple standard support and higher data throughput differentiates this solution from competitive products [3].

Each DSP core can perform up to 8000 MIPS or 8000 16b MMACs per second. A core has 8 functional units, 2 register files, 2 load/store data paths, 32KB of L1 instruction, and 32KB data-configurable SRAM/cache with ECC and memory protection. The 3MB L2 RAM is partitioned across the 3 cores and has ECC with memory protection. DSPs have full access to the memory map, all resources on the device, and can arbitrate over shared resources through direct signaling, or semaphores. Read, write, and execute restrictions to memory and chip-level components is enforced through memory protection hardware. The chip specifications are presented in Fig. 14.5.3.

The initial platform implementation is in a high-performance 65nm process with a 16-track MET2 library architecture using hierarchical Auto Place and Route (APR). The cell library has 2 V_t transistors, each with 2 channel length variants for performance-vs-leakage tradeoff. Extraction inaccuracy and driver sensitivity on short nets is significant below 90nm. A rich library to address these needs resulted in 6000 cells having been designed following [1].

A major implementation challenge in scaled processes is repeater insertion. As RC delay increases, the significance of cross-chip transport strategy is obvious. Device complexity is increasing as well as resulting in higher net count and near-optimal quality of results is required to avoid additional on-chip latencies. Wire width assignment and repeater insertion were simultaneously performed in an n-corner environment to address the slow/fast path timing closure problems across the entire design space. Network planning and non-critical net detouring was automated.

To meet core performance objectives, the gap between APR quality and full-custom, manual placement had to be narrowed. A new in-situ Regularized Placement (RP) technology was developed for this [2]. Placement constraints were automatically generated from generic structured RTL. Cells are regularly placed and sized simultaneously with non-RP cells. Sizing and realignment are continually updated as their environment changes. Alignment is maintained either on a common edge or on a specific signal as shown in Fig. 14.5.4 for leaf-level clockgating. In addition RP was applied to relieve routing congestion in targeted areas.

Clock gating is extensively used with 23k clock gates. Clock distribution uses cross-process balanced trees to reduce power with low insertion delay. Clock buffers, clock gates and delay buffers have transistor layout and sizing tuned to minimize both global and local variation. Clock routing is restricted to be matched with routing geometry selected for tracking and delay matching. The clock architecture is designed to push clock divergence down the tree to reduce on-chip variation. Structured placement is used on the clock for register clustering to reduce systemic skew by matching delay components within each clock cluster.

Customer board constraints impose a strict power budget for the chip. Simultaneously, customer product positioning requires best-in-class clock rates. An adaptive voltage scaling technique was developed for this device to counteract the nonlinear leakage power increase with increased I_{ds} strength of the transistor.

For each device, the minimum operating voltage to meet the required performance is determined during manufacturing test for two temperatures. The two voltages are then stored on the chip using fuses. These values are used by an external regulator to provide the optimal supply voltage. In low-voltage deep-submicron CMOS the circuit speed increases with temperature. So at high temperature an on-chip thermal diode signals a drop in supply voltage as shown in Fig. 14.5.5.

Test cost is a major challenge in determining the optimal supply voltage for each chip. On-chip variation in multi-core devices presents challenges to realize maximum voltage scaling. A technique was developed that enables rapid determination of the minimum chip operating voltage. Statistical simulations of various ring oscillators (ROs) and a wide variety of critical paths were performed. The delays of different RO sets were fitted to the critical path delays using a second order model where *D()* are the various delays, and a_i and b_{ij} are fitting parameters:

$$D(criticalpath) = \sum_i a_i D(RO_i) + \sum_{i,j} b_{ij} D(RO_i) D(RO_j)$$

The ROs having non-redundant information about the critical path performance were identified (Fig.14.5.6). Sets of these ROs were scattered on the die near critical paths to address systematic cross-die variation. Post-silicon characterization is used to build the fitting model and continuous updates are done to account for long-term process change. This technique can be used with a dynamically adjusted supply voltage with the model computed on-chip. A micrograph of the die is presented in Fig. 14.5.7.

References:

[1] C. Bittlestone, et al., "Architecting ASIC Libraries and Flows in the nm Era", *Design Automation Conference*, pp. 776 – 781, June, 2003.
[2] A. Hill, et al., "Physical Datapath: Regularized Datapath Placement and Optimization Technology," SNUG, March, 2005.
[3] Freescale MSC 8144 DSP,
http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MSC8144

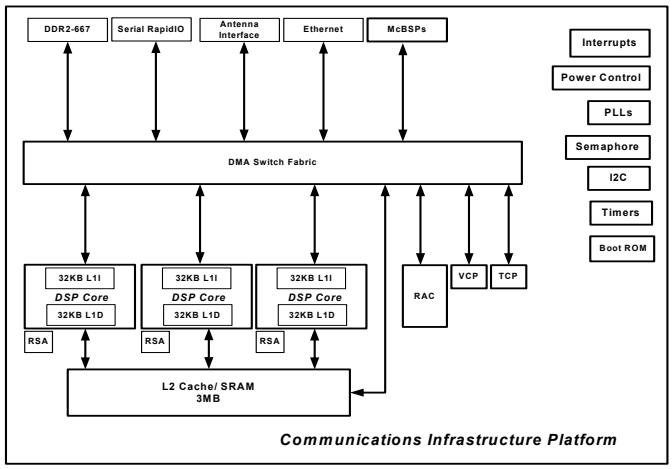

Figure 14.5.1: Communications Infrastructure Platform.

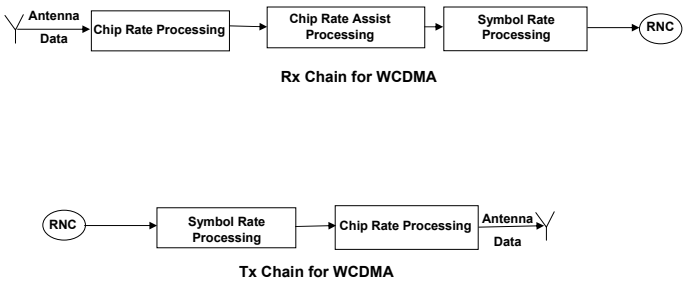

Figure 14.5.2: WCDMA signal chain.

Process	**65nm 7LM**
Frequency	**1.1 GHz**
Voltage Range	**0.9V-1.1V**
Power Dissipation	**6W**
Transistors	**300M**
Memory	**3MB L2** **32Kx3 L1I** **32Kx3 L1D**
Die Size	**130 mm²**

Figure 14.5.3: Chip Specifications.

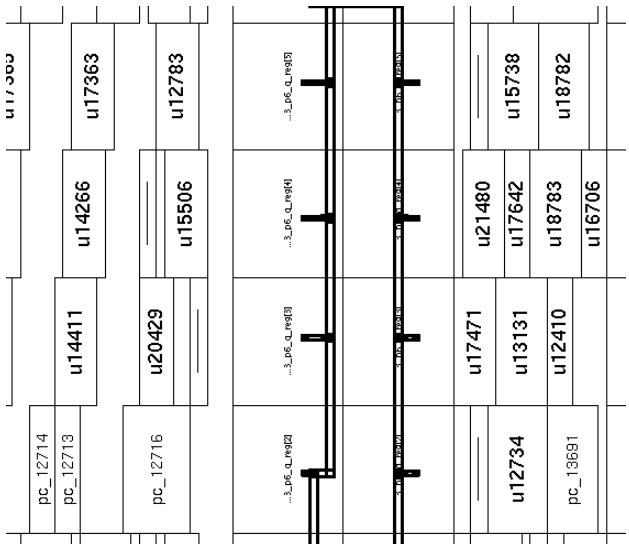

Figure 14.5.4: RP clockgating embedded within APR environment.

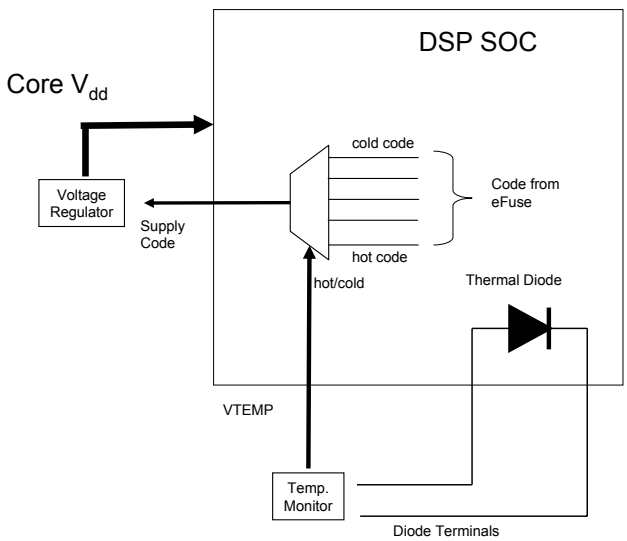

Figure 14.5.5: Adaptive supply voltage scheme for constant performance.

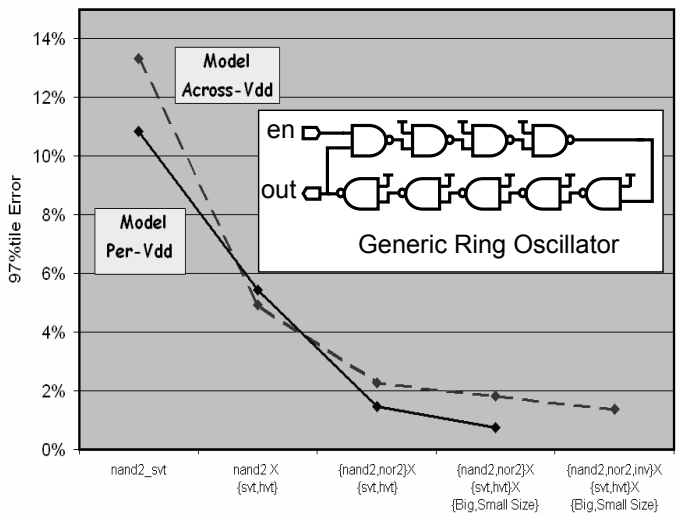

Figure 14.5.6: Error in critical path delay predictions for different ring oscillators.

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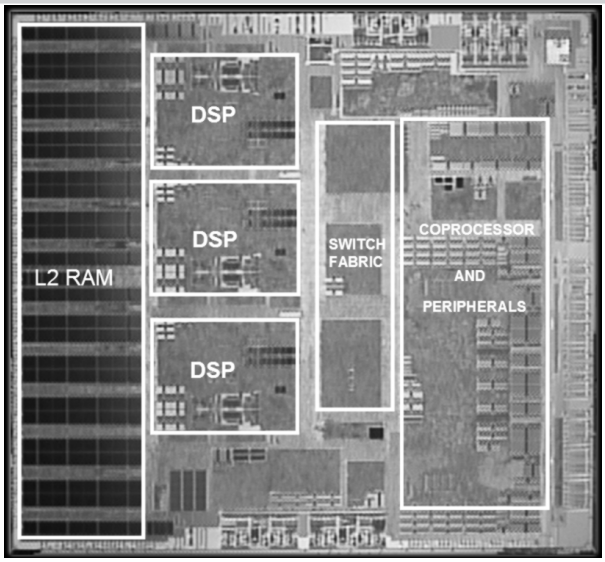

Figure 14.5.7 Die micrograph.

